

S/N 10/028,001

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al. Examiner: Tu-Tu V. Ho
Serial No.: 10/028,001 Group Art Unit: 2818
Filed: December 20, 2001 Docket: 1303.035US1
Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL
DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

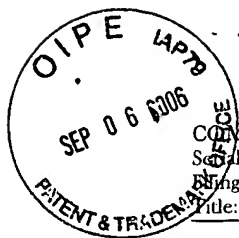
COMMUNICATION CONCERNING RELATED APPLICATIONS

MS Issue Fee

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date/Issue Date</u>	<u>Attorney Docket</u>	<u>Title</u>
11380599	April 27, 2006	1303.045US3	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
11471008	June 20, 2006	1303.035US3	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
11471007	June 20, 2006	1303.035US4	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
11471348	June 20, 2006	1303.035US5	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
11492638	July 25, 2006	1303.019US4	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
11492637	July 25, 2006	1303.019US5	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS



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Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

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By Marvin L. Beekman

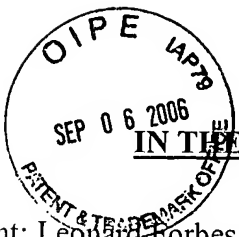
Marvin L. Beekman

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KATHLEEN E. ROTHROCK
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Kathleen E. Rothrock
Signature



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND
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Docket No.: 1303.035US1

Filed: December 20, 2001

Examiner: Tu-Tu V. Ho

Customer No.: 21186

Serial No.: 10/028,001

Due Date: September 5, 2006

Group Art Unit: 2818

Confirmation No.: 2627

Commissioner for Patents

Attn: MAIL STOP ISSUE FEE

P.O. Box 1450

Alexandria, VA 22313-1450

Notice of Allowance Date:

June 2, 2006

We are transmitting herewith the attached:

- ☒ A check in the amount of \$1400.00 to cover the Large Entity Issue Fee Payment
- ☒ A check in the amount of \$9.00 to cover the Extra Patent Copies Fee (3 copies)
- ☒ Issue Fee Transmittal (Form PTOL-85)
- ☒ Communication Re: Fee Address (1 pg)
- ☒ A check in the amount of \$300.00 to cover the Publication Fee Payment.
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- ☒ Communication Concerning Related Applications (2 pgs)

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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